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LISTING OF CLAIMS:

1. (Currently amended) A semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU, the device comprising:

a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal; and

an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit,

wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and

wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal.

2. (Currently amended) The semiconductor integrated circuit device according to claim 1, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit, a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU, progress of an operation of the functional circuit until completion of processing that is performed in response to

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the break request, and a setting information storage circuit for storing setting information indicating whether to enable or disable an operation stop function of the stop control circuit; and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are constructed to be reset by the second reset signal but not by the first reset signal.

3. (Currently amended) The semiconductor integrated circuit device according to claim 1, further comprising:

an emulation memory for storing a user program that is executed by the CPU in response to the first reset signal; and

a monitor program memory for storing a monitor program that is executed by the CPU in response to the second reset signal.

4. (Original) The semiconductor integrated circuit device according to claim 1, wherein:

the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode; and

a break request control circuit is provided for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode.

5. (Original) The semiconductor integrated circuit device according to claim 4, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break request signal is input in a period when the CPU is in the normal operation rode, and outputs a break request signal to the CPU upon input of the wake-up signal if the break

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request signal is input in a period when the CPU is in the low power consumption operation mode.

6. (Original) The semiconductor integrated circuit device according to claim 4, further comprising:

a break request control register that is reset by the second reset signal,

wherein the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register.

7. (Original) The semiconductor integrated circuit device according to claim 4, further comprising:

a wake-up signal generation circuit for generating awake-up signal when a prescribed set time has elapsed from a transition of the CPU from the normal operation mode to the low power consumption operation mode.

8. (Original) The semiconductor integrated circuit device according to claim 7, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode;

a storage circuit for storing a set count corresponding to the set time; and

a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count.

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9. (Currently amended) A microcomputer development assisting apparatus comprising:

a semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU in a state that the semiconductor integrated circuit device is electrically connected, in place of the one-chip microcomputer, to a circuit board to be mounted with the one-chip microcomputer; and

a host for setting a condition of emulation by the semiconductor integrated circuit device and for performing data processing on an emulation result,

wherein the semiconductor integrated circuit device includes

a CPU;

a peripheral circuit that is controlled by the CPU;

a vector address switching circuit for outputting a vector address of a user program corresponding to a reset vector address supplied from the CPU when receiving a first reset signal from the circuit board, and for outputting a vector address of a monitor program instead-of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal from the host, and

an interface circuit for performing input and output of information relating to the emulation between the CPU and an external circuit,

wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and

wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal.

10. (Currently amended) The microcomputer development assisting apparatus according to claim 9, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit, a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU, progress of an operation of the functional circuit until completion of processing that is performed in response to the break request, and a setting information storage circuit for storing setting information indicating whether to enable or disable an operation stop function of the stop control circuit; and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are constructed to be reset by the second reset signal but not by the first reset signal.

11. (Currently amended) The microcomputer development assisting apparatus according to claim 9, wherein the semiconductor integrated circuit device further includes:

an emulation memory for storing a user program that is executed by the CPU in response to the first reset signal; and

a monitor program memory for storing a monitor program that is executed by the CPU in response to the second reset signal.

12. (Original) The microcomputer development assisting apparatus according to claim 9, wherein:

the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode; and

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the semiconductor integrated circuit device further includes a break request control circuit for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode.

13. (Original) The microcomputer development assisting apparatus according to claim 12, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break request signal is input in a period when the CPU is in the normal operation mode, and outputs a break request signal to the CPU upon input of the wake-up signal if the break request signal is input in a period when the CPU is in the low power consumption operation mode.

14. (Original) The microcomputer development assisting apparatus according to claim 12, wherein:

the semiconductor integrated circuit device further includes a break request control register that is reset by the second reset signal; and

the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register.

15. (Original) The microcomputer development assisting apparatus according to claim 12, wherein the semiconductor integrated circuit device further includes a wake-up signal generation circuit for generating a wake-up signal when a prescribed set time has elapsed from a

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transition of the CPU from the normal operation mode to the low power consumption operation mode.

16. (Original) The semiconductor integrated circuit device according to claim 15, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode;

a storage circuit for storing a set count corresponding to the set time; and

a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count.

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